

SEMBODAI RUKMANI VARATHARAJAN ENGINEERING COLLEGE SEMBODAI – 614809

(Approved By AICTE, Newdelhi – Affiliated To ANNA UNIVERSITY:: Chennai)

EC6411 CIRCUITS AND SIMULATION INTEGRATED LABORATORY

(REGULATION-2013)

LAB MANUAL DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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(REGULATION 2013) AS PER ANNA UNIVERSITY SYLLABUS

SYLLABUS

LIST OF EXPERIMENTS:

DESIGN AND ANALYSIS OF;

- 1. Series and Shunt feedback amplifiers-Frequency response, Input and output impedance calculation
- 2. RC Phase shift oscillator and Wien Bridge Oscillator
- 3. Hartley Oscillator and Colpitts Oscillator
- 4. Single Tuned Amplifier
- 5. RC Integrator and Differentiator circuits
- 6. Astable and Monostable multivibrators
- 7. Clippers and Clampers
- 8. Free running Blocking Oscillators

SIMULATION USING SPICE:

- 1. Tuned Collector Oscillator
- 2. Twin -T Oscillator / Wein Bridge Oscillator
- 3. Double and Stagger tuned Amplifiers
- 4. Bistable Multivibrator
- 5. Schmitt Trigger circuit with Predictable hysteresis
- 6. Monostable multivibrator with emitter timing and base timing
- 7. Voltage and Current Time base circuits

B.E (ELECTRONICS & COMMUNICATION ENGINEERING)

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		Series and Shunt feedback amplifiers-			
1		Frequency response, Input and output			
		impedance Calculation			
2		Wien Bridge Oscillator			
		RC Phase shift oscillator			
3		Hartley Oscillator and Colpitts Oscillator			
4		Single Tuned Amplifier			
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7		Clippers and Clampers			
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		CYCLE – II		1	
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EX.NO: FEED BACK AMPLIFIERS

DATE:

AIM:

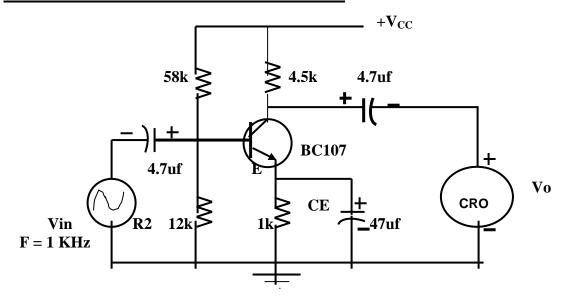
To design and test the current series and voltage shunt Feedback Amplifier and to calculate the following parameters with and without feedback.

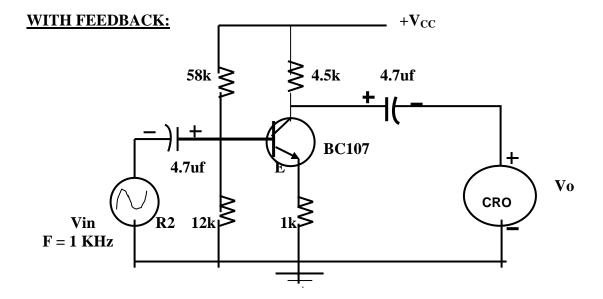
- 1. Mid band gain.
- 2. Bandwidth and cutoff frequencies.
- 3. Input and output impedance.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR		1
3	CAPACITOR	4.7uf ,	2,
		47uf	1
4	CRO	(0-30)MHz	1
5	RPS	(0-30) V	1
6	FUNCTION	(0-1)MHZ	1
	GENERATOR		

CIRCUIT DIAGRAM: WITHOUT FEEDBACK:





CURRENT SERIES FEEDBACK

DESIGN: (Without Feedback):

Given data :
$$Vcc = 15V$$
, $\beta = 0.9$, $f_L = 1kHz$, $Ic=1mA$. Stability factor = [2-10], $Rs = 680\Omega$,

$$Av = 50dB$$
, $I_E = 1.2mA$.

Gain for3mula is given by

$$Av = -hfe R_{Leff} / Z i$$

Assume,

$$V_{CE} = Vcc / 2$$

$$R_{Leff} = Rc$$

$$re = 26mV / I_E$$

hie = β re where re is internal resistance of the transistor.

hie = hfe re

$$VE = Vcc / 10$$

On applying KVL to output loop,

$$\mathbf{Vcc} = \mathbf{I_cR_c} + \mathbf{V_{CE}} + \mathbf{I_ER_E}$$

$$V_E = I_E R_E$$

$$Rc = ?$$

Since I_B is very small when compared with IC

Ic approximately equal to I_E

$$\mathbf{R}_{\mathbf{E}} = \mathbf{V}_{\mathbf{E}} / \mathbf{I}_{\mathbf{E}} = \mathbf{?}$$

$$\mathbf{V_B} = \mathbf{V_{BE}} + \mathbf{V_E}$$

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$$\begin{split} V_B &= V_{CC} \cdot R_{B2} / R_{B1} + R_{B2} \\ S &= 1 + (R_B / R_E) \\ R_B &= ? \\ R_B &= R_{B1} R_{B2} \end{split}$$

Find

Input Impedance, $Zi = (R_B \text{ hie})$

Coupling and bypass capacitors can be thus found out.

Input coupling capacitor is given by , $X_{ci} = Z_i / 10$

$$Xci = 1/2\pi fC_i$$

 $Ci = ?$

output coupling capacitor is given by,

$$X_{co} = (Rc RL) / 10$$

$$Xc_0 = 1 / 2\pi fC_0$$

$$C_0 = ?$$

By-pass capacitor is given by $X_{CE} = 1/2\pi f C_E$

$$C_E = ?$$

Design (With feedback):

Remove the emitter capacitance (C_E)

$$\begin{split} \beta &= \text{-}1 \ / \ R_E \\ Gm &= \ \text{-} \ h_{fe} / \left[(hie + R_E \) \ R_B \right] \ \Big| \\ D &= 1 + \beta \ G_m \\ G_{mf} &= \ G_m / \ D \\ Z_{if} &= Z \ _i D \\ Z_{of} &= Z_o D \end{split}$$

Voltage shunt DESIGN: (Without Feedback):

Given data : Vcc = 15V ,
$$f_L$$
 = 1kHz, Ic=1mA.
 Stability factor = [2-10], Rs = 680 Ω ,
 Av =40 dB .

Gain formula is given by

$$Av = -hfe R_{Leff} / Z i$$

Assume,
$$V_{CE} = Vcc / 2$$

$$R_{Leff} = R c | RL$$

$$re = 26mV / I_E$$

hie = β re where re is internal resistance of the transistor.

hie = hfe re

$$VE = Vcc / 10$$

On applying KVL to output loop,

$$\mathbf{Vcc} = \mathbf{I_cR_c} + \mathbf{V_{CE}} + \mathbf{I_ER_E}$$

$$V_E = I_E R_E$$

$$Rc = ?$$

Since I_B is very small when compared with I_C

Ic approximately equal to I_E

$$R_E = V_E / I_E = ?$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{\rm CC}$$
 . $R_{\rm B2}$ / $R_{\rm B1}$ + $R_{\rm B2}$

$$S = 1 + R_B / R_E$$

$$R_R = ?$$

$$R_B = R_{B1} || R_{B2}$$

Find

Input Impedance, $Zi = (R_B \parallel hie)$

Coupling and bypass capacitors can be thus found out.

Input coupling capacitor is given by , $X_{ci} = Z_i / 10$

$$Xci = 1/2\pi f C_i$$

$$Ci = ?$$

output coupling capacitor is given by,

$$X_{co}=(Rc \mid RL)/10$$

$$Xc_0 = 1/2\pi f C_0$$

$$C_0 = ?$$

By-pass capacitor is given by, X_{CE} = 1/2 π f C_E

$$C_E = ?$$

Design (With feedback):

Connect the feedback resistance (Rf) and feedback capacitor (Cf) as shown in the figure.

$$Xcf = R_f / 10$$

$$C_f = R_f / 2\pi f \times 10$$

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Assume, $Rf = 68 K\Omega$

$$\beta = -1 / R_f$$

 $Trans-resistance \ Rm=-\ h_{fe}\left(RB\right|\mid Rf\)\ (Rc\mid\mid Rf\)\ /\ (RB\mid\mid Rf\)+hie$

$$D = 1 + \beta Rm$$

$$Avf = Rmf / Rs$$

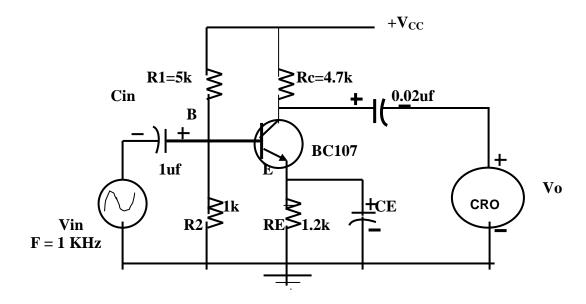
$$Rmf = Rm / D$$

$$\mathbf{Z_{if}} = \mathbf{Zi} / \mathbf{D}$$

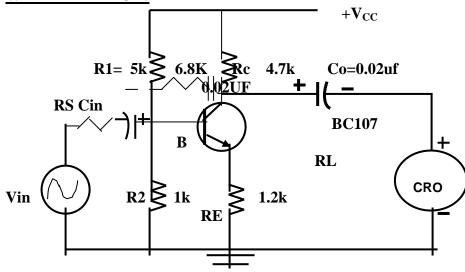
$$\mathbf{Z}_{of} = \mathbf{Z}_{o} / \mathbf{D}$$

CIRCUIT DIAGRAM: Voltage shunt feedback

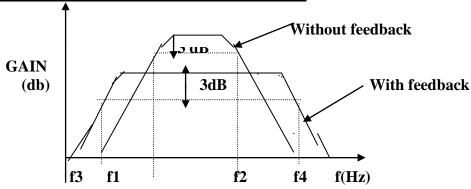
WITHOUT FEEDBACK:



WITH FEEDBACK:



MODEL GRAPH(WITH & WITHOUT FEEDBACK)



f2 - f1 = Bandwidth of without feedback circuit

f4 - f3 = Bandwidth of with feedback circuit

THEORY:

An amplifier whose function fraction of output is fed back to the input is called feed back amplifier. Depending upon whether the input is in phase or out of phase with the feed back signal, they are classified in to positive feed back and negative feed back. If the feed back signal is in phase with the input, then the wave will have positive gain. Then the amplifier is said to have a positive feed back.

If the feed back signal is out of phase with the input ,then the wave will have a negative gain. The amplifier is said to have a negative feed back. The values of voltage gain and bandwidth without feed back.

PROCEDURE:

The connections are made as shown in the circuit. The amplifier is checked for its correct operation .Set the input voltage to a fixed value. Keeping the input voltage Vary the input frequency from 0Hz to 1MHz and note down the corresponding output voltage. plot the graph: gain (dB) vs frequency .Find the input and output impedances. Calculate the bandwidth from the graph. Remove RE and follow the same procedure.

OBSERVATION:

WITH OUT FEEDBACK

Vin = ----- **Volts**

S.NO	FREQUNCY	O/P voltage Vo	Gain
			Av=20 log Vo/Vi

WITH FEEDBACK

	WITH EEDDITCH					
S.NO	FREQUNCY	O/P voltage	Av=20 log Vo/Vi			

RESULT:

Theoritical

Practical

	With F/B	Without F/B	With F/B	Without F/B
Input Impedance				
Output				
Impedance				
Bandwidth				
Transconductance				
(gm)				

EX.NO: RC PHASE SHIFT OSCILLATOR

DATE:

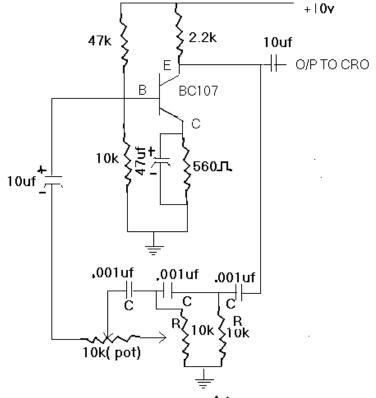
AIM:

To design and construct the transistor Phase shift oscillator.

APPARATUS REQUIRED:

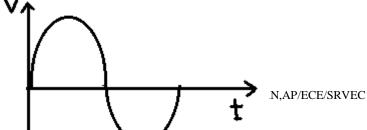
S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR		
3	CAPACITOR		
4	CRO	(0-30) MHz	1
5	RPS	(0-30) V	1
6	FUNCTION	(0-1)MHz	1
	GENERATOR		

CIRCUIT DIAGRAM:



MODEL GRAPH:

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DESIGN:

Given : Vcc = 12V , fo = 1 KHz,C = 0.01 µF;
$$I_E$$
 = 5mA.; Stability factor = 10
$$f = 1/2\pi RC \quad Find \ R$$

$$R1 = (Ri - R)$$

$$R >> Rc$$

$$Beta = -1/29$$

Amplifier Design:

Gain formula is given by

$$Av = -hfe R_{Leff} / hie (Av = 29, design given)$$

Assume,
$$V_{CE} = Vcc / 2$$

$$R_{Leff} = R c | RL$$

$$re = 26mV / I_E$$

hie = β re where re is internal resistance of the transistor.

hie = hfe re

$$VE = Vcc / 10$$

On applying KVL to output loop,

$$\mathbf{Vcc} = \mathbf{I_c}\mathbf{R_c} + \mathbf{V_{CE}} + \mathbf{I_E}\mathbf{R_E}$$

$$V_E = I_E R_E$$

$$Rc = ?$$

Since I_B is very small when compared with Ic

Ic approximately equal to I_E

$$\mathbf{R}_{\mathbf{E}} = \mathbf{V}_{\mathbf{E}} / \mathbf{I}_{\mathbf{E}} = \mathbf{?}$$

$$\mathbf{V}_{\mathbf{B}} = \mathbf{V}_{\mathbf{B}\mathbf{E}} + \mathbf{V}_{\mathbf{E}}$$

$$\mathbf{V}_{\mathrm{B}} = \mathbf{V}_{\mathrm{CC}} \cdot \mathbf{R}_{\mathrm{B2}} / \mathbf{R}_{\mathrm{B1}} + \mathbf{R}_{\mathrm{B2}}$$

$$S = 1 + R_B / R_E$$

$$R_R = ?$$

$$R_B = R_{B1} || R_{B2}$$

Find RB1 & RB2

Input Impedance, $Zi = (R_B \parallel hie)$

Coupling and bypass capacitors can be thus found out.

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Input coupling capacitor is given by , $X_{ci} = Z_i / 10$

$$Xci = 1/2\pi f C_i$$

$$Ci = ?$$

output coupling capacitor is given by,

$$Xc_0 = 1/2\pi f C_0$$

$$C_0 = ?$$

By-pass capacitor is given by, $X_{CE} = 1/2\pi f C_E$

$$C_E = ?$$

THEORY:

The Transistor Phase Shift Oscillator produces a sine wave of desired designed frequency. The RC combination will give a 60° phase shift totally three combination will give a 180° phase shift. The BC107 is in the common emitter configuration. Therefore that will give a 180° phase shift totally a 360° phase shift output is produced. The capacitor value is designed in order to get the desired output frequency. Initially the C and R are connected as a feedback with respect to input and output and this will maintain constant sine wave output. CRO is connected at the output.

PROCEDURE:

- 1. The circuit is constructed as per the given circuit diagram.
- 2. Switch on the power supply and observe the output on the CRO(sine wave)
- 3. Note down the practical frequency and compare it with the theoretical frequency.

RESULT:

	Theoritical	Practical
Frequency	$f = 1/2 \Pi RC \sqrt{6RC}$	

EX.NO: WEIN BRIDGE OSCILLATOR

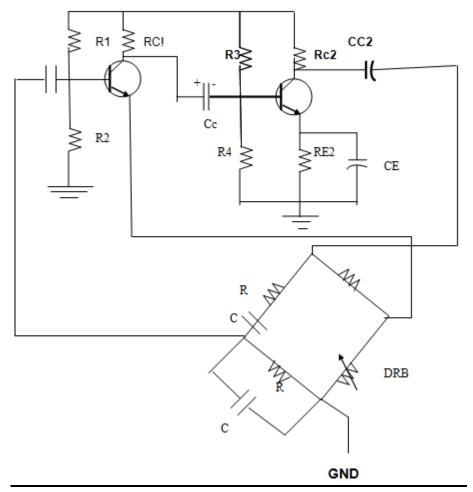
DATE:

Aim: To Design and construct a Wein – Bridge Oscillator for a given cut-off frequency.

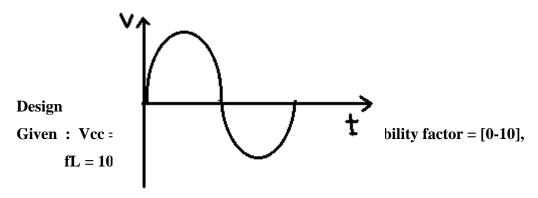
APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC107	2
2	RESISTOR		
3	CAPACITOR		
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

CIRCUIT DIAGRAM:



MODEL GRAPH:



When the bridge is balanced,

$$fo = 1/2\pi RC$$

Assume, $C = 0.1 \mu F$

Find, fo = ?

Given data : Vcc = 15V, $f_L = 50Hz$, $I_{c1} = I_{c2} = 1mA$.; $A_{vT} = 3$; Av1 = 2; Av2 = 1;

Stability factor = [10]

Gain formula is given by

$$Av = -hfe R_{Leff} / Zi$$

$$R_{Leff} = R c_2 || RL$$

 $hfe_2 = 200$ (from multimeter)

$$re_2 = 26mV / I_{E2} = 26$$

$$hie_2 = hfe_2 re_2 = 200 x 26 = 5.2kW$$

From dc bias analysis, on applying KVL to the outer loop, we get

$$\mathbf{Vcc} = \mathbf{I}_{c2}\mathbf{R}_{c2} + \mathbf{V}_{CE2} + \mathbf{V}_{E2}$$

$$V_{cE2} = Vcc/2$$
; $V_{E2} = Vcc / 10$; $I_{c2} = 1mA$

$$\mathbf{Rc}_2 = ?$$

Since I_B is very small when compared with I_C

Ic approximately equal to I_E

$$Av_2 = -hfe_2 R_{Leff} / Zi_2$$

Find RL|| Rc2 from above equation

Since Rc2 is known, Calculate RL.

$$V_{E2} = I_{E2}R_{E2}$$

Calculate R_{E2}

$$S = 1 + R_{B2} / R_{E2}$$

$$R_{B2} = ?$$

$$R_{B2} = R3 || R4$$

$$V_{B2} = V_{CC} \cdot R4 / R3 + R4$$

$$\mathbf{V}_{\mathbf{B2}} = \mathbf{V}_{\mathbf{BE2}} + \mathbf{V}_{\mathbf{E2}}$$

$$R3 = ?$$

Find R4

$$Zi2 = (R_{B2} \parallel hie2)$$

$$Zi2 = ?$$

$$R_{leff1} = Zi2 || Rc1$$

Find R_{leff1} from the gain formula given above

$$Av1 = -hfe1 R_{Leff 1} / Zi1$$

$$\mathbf{R}_{\mathbf{Leff1}} = ?$$

On applying KVL to the first stage, we get

$$\mathbf{Vcc} = \mathbf{Ic_1} \ \mathbf{Rc_1} + \mathbf{V_{CE1}} + \mathbf{V_{E1}}$$

$$V_{CE1} = VCC / 2$$
; $V_{E1} = VCC / 10$

$$Rc1 = ?$$

Find Ic1 approximately equal to I_{E1}

$$R6 = RE1 = ?$$

$$S = 1 + R_{B1} / R_{E1}$$

$$R_{B 1} = ?$$

$$R_{B1} = R1 || R2$$

$$V_{B1} = V_{CC} \cdot R2 / R1 + R2$$

$$VB1 = VBE2 + VE2$$

Find R1 = ?

Therefore find R2 = ?

$$\mathbf{Zi1} = (\mathbf{R}_{\mathbf{B1}} \parallel \mathbf{hie1})$$

$$R5 = RL - R6$$

Coupling and bypass capacitors can be thus found out.

Input coupling capacitor is given by , $X_{ci} = Z_i / 10$

$$Xci = 1/2\pi f C_i$$

$$Ci = ?$$

output coupling capacitor is given by,

$$X_{co} = (Rc_2 | | RL_2) / 10$$

$$Xc_0 = 1/2\pi f C_0$$

$$C_0 = ?$$

By-pass capacitor is given by, $X_{CE} = R_{E2} / 10$

$$X_{CE}$$
 1/2 π f C_{E2}

$$C_E = ?$$

THEORY:

In wein bridge oscillator, wein bridge circuit is connected between the amplifier input terminals and output terminals. The bridge has a series rc network in one arm and parallel network in the adjoining arm. In the remaining 2 arms of the bridge resistors R1and Rf are connected . To maintain oscillations total phase shift around the circuit must be zero and loop gain unity. First condition occurs only when the bridge is balanced . Assuming that the resistors and capacitors are equal in value, the resonant frequency of balanced bridge is given by

$$F_0 = 0.159 RC$$

PROCEDURE:

- 1. The circuit is constructed as per the given circuit diagram.
- 2. Switch on the power supply and observe the output on the CRO(sine wave)
- 3. Note down the practical frequency and compare it with the theoretical frequency.

RESULT:

Theoritical	Practical
$f = 1/2 \Pi RC$	

EX.NO: HARTLEY and COLPITT OSCILLATOR

DATE:

AIM:

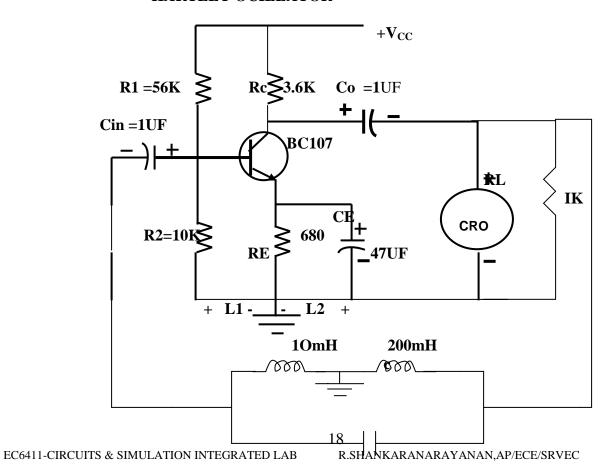
To Design and construct the given Oscillator at the given operating frequency.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR		1
3	CAPACITOR		
4	CRO	(0-30)MHZ	1
5	RPS	(0-30) V	1
6	FUNCTION	(0-1) MHz	1
	GENERATOR		
7	DIB, DRB		1

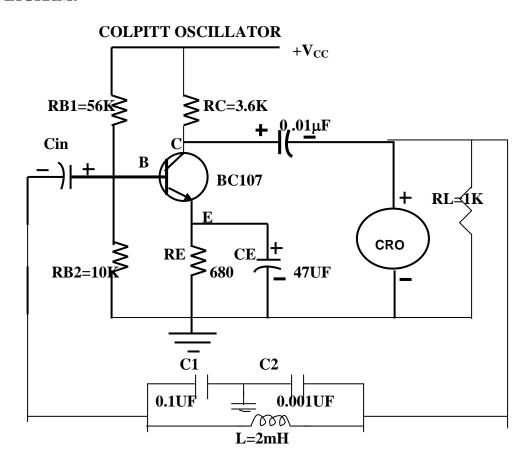
CIRCUIT DIAGRAM:

HARTLEY OCILLATOR

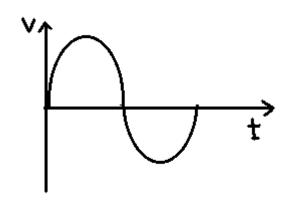


2 UF

CIRCUIT DIAGRAM:



MODEL GRAPH:



Design of Feedback Network (Hartely Oscillator):

$$Av = 1 / \beta = -L1 / L2$$

$$F = 1/2\pi\sqrt{(L1 + L2)C};$$
 $C = ?$

Design of Feedback Network (Colpitt Oscillator):

Given :
$$C1 = 0.1 \mu F; f = 800 kHz; \ Vcc = 12V \ ; \ Av = 50 \ ; \ S = 10$$

$$I_E = 5mA; \ fi = 1kHz$$

$$Av = Av = 1 \ / \ \beta = C2 \ / \ C1$$

$$f = 1/2\pi \sqrt{(C1 + C2) \ / \ LC1C2}$$

$$L = ?$$

Amplifier Design:

Gain formula is given by

$$Av = -hfe R_{Leff} / hie (Av = 29, design given)$$

Assume, $V_{CE} = Vcc / 2$

$$R_{Leff} = R c | RL$$

$$re = 26mV / I_E$$

hie = β re where re is internal resistance of the transistor.

hie = hfe re —

$$VE = Vcc / 10$$

On applying KVL to output loop,

$$\mathbf{Vcc} = \mathbf{I_cR_c} + \mathbf{V_{CE}} + \mathbf{I_ER_E}$$

$$V_E = I_E R_E$$

$$Rc = ?;RL = ?$$

Since I_B is very small when compared with Ic

Ic approximately equal to I_E

$$\mathbf{R}_{\mathbf{E}} = \mathbf{V}_{\mathbf{E}} / \mathbf{I}_{\mathbf{E}} = ?$$

$$\mathbf{V_B} = \mathbf{V_{BE}} + \mathbf{V_E}$$

$$V_B = V_{CC} \cdot R_{B2} / R_{B1} + R_{B2}$$

$$S = 1 + R_B / R_E$$

$$R_{\rm R} = ?$$

$$\mathbf{R}_{\mathbf{B}} = \mathbf{R}_{\mathbf{B}1} || \mathbf{R}_{\mathbf{B}2}$$

Find RB1 & RB2

Input Impedance, $Zi = (R_B \parallel hie)$

Coupling and bypass capacitors can be thus found out.

Input coupling capacitor is given by , $X_{ci} = Z_i / 10$

$$Xci = 1/2\pi f C_i$$

$$Ci = ?$$

output coupling capacitor is given by,

$$\mathbf{X}\mathbf{c}_0 = (\mathbf{R}\mathbf{c} \mid\mid \mathbf{R}\mathbf{L}) / 10$$

$$Xc_0 = 1/2\pi f C_0$$

$$C_0 = ?$$

By-pass capacitor is given by, $X_{CE} = R_E / 10$

$$X_{CE} = 1/2\pi f C_E$$

$$C_E = ?$$

THEORY:

LC oscillator consisting of a tank circuit for generating sine wave of required frequency. Rectifying Barkhausen criteria $A\beta$ for a circuit containing reactance $A\beta$ must be positive and greater than or equal to unity.

PROCEDURE:

- 1. The circuit connection is made as per the circuit diagram.
- 2. Switch on the power supply and observe the output on the CRO(sine wave).
- 3. Note down the practical frequency and compare it with the theoretical frequency.

THEORETICAL FREQUENCY FOR HARTLEY OSCILLATOR:

THEORETICAL FREQUENCY FOR COLPITT OSCILLATOR:

$$fc = 1/2\pi\sqrt{(C1 + C2)} / LC1C2$$

PRACTICAL:

Observed Values:

Time Period =

Frequency =

RESULT:

Thus the LC oscillator is designed for the given frequency and the output response is verified.

	Theoritical		Practical	
Frequency	Hartley	Colpitt	Hartley	Colpitt
1	3	F		P

EX.NO: CLASS "C" SINGLE TUNED AMPLIFIER

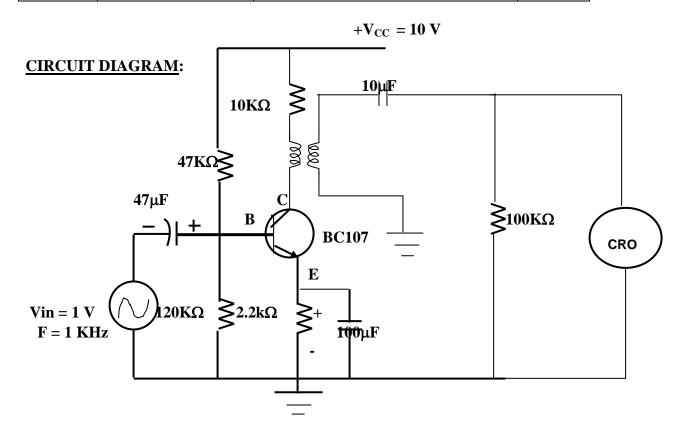
DATE:

AIM:

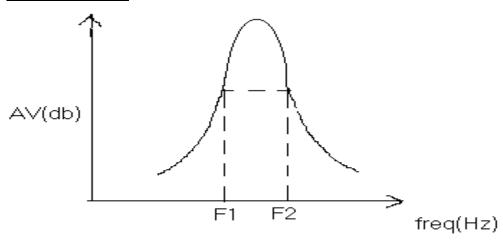
To study the operation of class c tuned amplifier.

APPARATUS REOUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR	4.2KΩ, 500 Ω, 197 KΩ, 2.2 KΩ,	1
3	CAPACITOR	0.1µf	2
		0.001µf, 100µf	1
4	CRO	-	1
5	RPS	(0-30) V	1
6	FUNCTION	-	1
	GENERATOR		



MODEL GRAPH:



THEORY:

The amplifier is said to be class c amplifier if the Q Point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle Due to such a selection of the Q point, transistor remains active for less than a half cycle. Hence only that much Part is reproduced at the output for remaining cycle of the input cycle the transistor remains cut off and no signal is produced at the output .the total

Angle during which current flows is less than 180°. This angle is called the conduction angle, Qc

PROCEDURE:

- 1. The connections are given as per the circuit diagram.
- 2. Connect the CRO in the output and trace the waveform.
- **3.**calculate the practical frequency and compare with the theoretical Frequency
- 4.plot the waveform obtained and calculate the bandwidth

RESULT:

Thus a class c single tuned amplifier was designed and its bandwidth is Calculated.

EX.NO: INTEGRATOR

DATE: AIM:

To study the output waveform of integrator.

APPARATUS REQUIRED:

APPARATUS NAME	RANGE	QUANTITY
AUDIO OSCILLATOR CRO RESISTORS CAPACITOR OP-AMP BREADBOARD RPS	1K,10K 0.1μF IC741	1 1 1 1 1

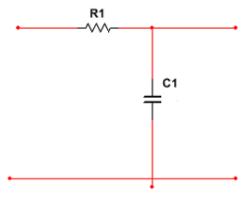
THEORY:

A simple low pas RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However in the op-amp integrator by MILLER's theorem, the effective input capacitance becomes C_f (1-A_v), where A_v is the gain of the op-amp. The gain A_v is the infinite for an ideal op-amp, so the effective time constant of the opamp integrator becomes very large which results perfect integration.

PROCEDURE:

- 1. Connections are given as per the circuit diagram.
- 2. The resistance R_{comp} is also connected to the (+) input terminal to minimize the effect of the input bias circuit.
- 3.It is noted that the gain of the integrator decreases with increasing frequency.
- **4.**Thus the integrator circuit does not have any high frequency problem.

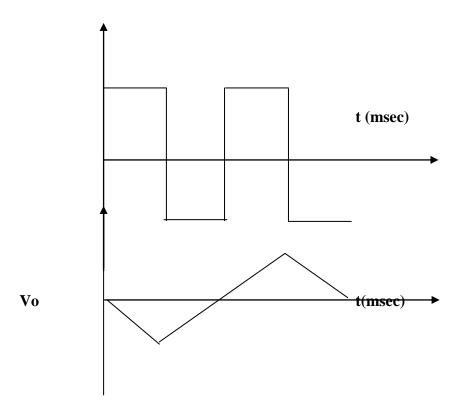
CIRCUIT DIAGRAM:



R1=1K; C1=1UF

MODEL GRAPH:

Vi



RESULT:- Thus the integrator using op-amp is studied.

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EX.NO: CLIPPER & CLAMPER CIRCUITS

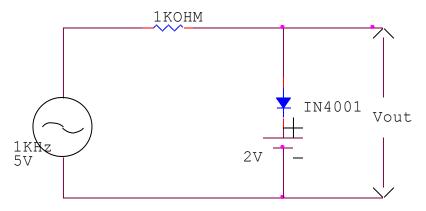
DATE:

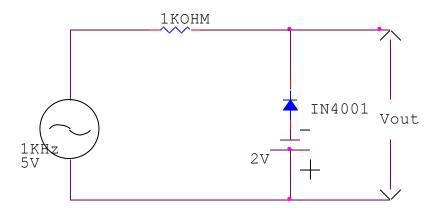
AIM: To observe the clipping waveform in different clipping configurations.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	DIODE	IN4001	1
2	RESISTOR	1ΚΩ	1
		10 ΚΩ	1
3	CAPACITOR	0.1μF	1
4	FUNCTION GENERATOR	(0-1) MHz	1
5	CRO	-	1

CLIPPER CIRCUIT DIAGRAM:





Procedure:

- 1. Connections are given as per the circuit.
- 2. Set input signal voltage (5v,1kHz) using function generator.
- 3. Observe the output waveform using CRO.
- 4. Sketch the observed waveform on the graph sheet.

(b) CLAMPING CIRCUITS

Aim:

To study the clamping circuits

(a). Positive clamper circuit (b) Negative clamper circuit

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	DIODE	IN4001	1
2	RESISTOR	1ΚΩ	1
		10 ΚΩ	1
3	CAPACITOR	0.1μF	1
4	FUNCTION GENERATOR	(0-1) MHz	1
5	CRO	-	1

DESIGN:

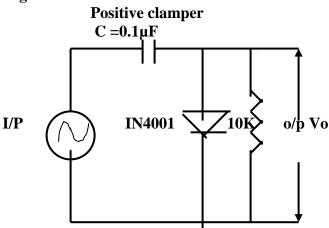
Given
$$f = 1kHz$$

$$T = 1 / f = 1x \cdot 10^{-3} \text{ Sec RC}$$

Assuming, $C = 0.1 \mu\text{F}$

$$R = 10 \text{ K}\Omega$$

Circuit Diagram:

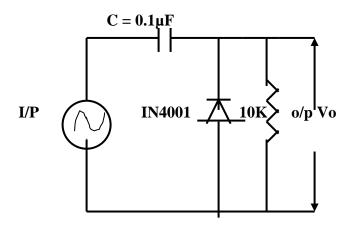


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Negative clamper



Procedure:

- 1. Connections are given as per the circuit .
- 2. Set input signal voltage (5v,1kHz) using function generator.
- 3. Observe the output waveform using CRO.
- 4. Sketch the observed waveform on the graph sheet.

Result:

Thus the waveforms are observed and traced for clipper and clamper circuits .

EX.NO: MONOSTABLE MULTI VIBRATOR

DATE:

AIM:

To Design the monostable multivibrator and plot the waveform.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	9ΚΩ	1
3	CAPACITOR	0.01μF	1
		0.1μF	1
4	RPS	(0-30) V	1
5	CRO	-	1

THEORY:

A monostable multivibrator has one stable state and a quasistable state. When it is triggered by an external agency it switches from the stable state to quasistable state and returns back to stable state. The time during which it states in quasistable state is determined from the time constant RC. When it is triggered by a continuous pulse it generates a square wave. Monostable multi vibrator can be realized by a pair of regeneratively coupled active devices, resistance devices and op-amps.

DESIGN:

Given
$$Vcc = 12V$$
; $V_{BB} = -2V$; $Ic = 2$ mA; $V_{CE(sat)} = 0.2$ V; $h_{FE} = 200$; $f = 1$ kHz.
$$R_C = V_{CC} - V_{CE(sat)} / I_C = 12 - 0.2 / 2 \times 10^{-3} = 5.9 \text{ K}\Omega$$

$$I_{B 2}(min) = I_{c2} / h_{fe} = 2$$
mA $/ 200 = 10 \text{ }\mu\text{A}$
$$Select \ I_{B 2} > I_{B 1}(min) \ (say \ 25 \text{ }\mu\text{A})$$

$$Then \ R = V_{CC} - V_{BE(sat)} / I_{B 2} = 12 - 0.7 / 25 \times 10^{-6} = 452 \text{ K}\Omega$$

$$T = 0.69 \text{ RC}$$

$$1 \times 10^{-3} = 0.69 \times 452 \times 10^{-3} \text{ C}$$

$$C = 3.2 \text{ nF}$$

$$V_{B1} = V_{BB} R1 / R1 + R2 + V_{CE(sat)} R2 / R1 + R2$$
 Since Q1 is off state, VB1 less than equal to 0.
$$Then \ V_{BB} R1 / R1 + R2 = V_{CE(sat)} R2 / R1 + R2$$

$$V_{BB} R1 = V_{CE(sat)} R2$$

2R1 = 0.2R2

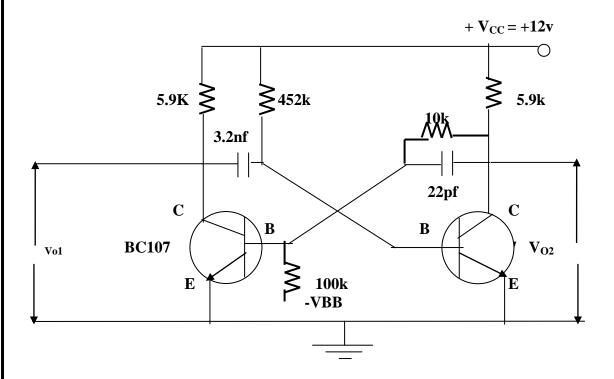
Assume $R1 = 10 \text{ K}\Omega$. Then $R2 = 100 \text{ K}\Omega$

C1 = 25pF(Commutative capacitor)

procedure:

- 1. Connect the circuit as per circuit diagram.
- 2. Switch on the regulated power supply and observe the output waveform at the collector of Q1 and Q2 and plot it.
- 3. Trigger the monostable multivibrator with a pulse and observe the change in waveform.
- 4. Plot the waveform and observe the changes before and after triggering the input to the circuit.

CIRCUIT DIAGRAM:



PROCEDURE:

The connections are made as per the diagram. The value of R is chosen as $9k\Omega$. The DCB is set to the designed value. The power supply is switched on and set to +5V. The output of the pulse generator is set to the desired frequency. Here the frequency of triggering should be greater than width of ON period (i.e.) T >W. The output is observed using CRO and the result is compared with the theoretical value. The experiment can be repeated for different values of C and the results are tabulated.

OBSERVATION

C (uf)	Theoritical(T=1.095 RC(ms)))	Practical T(ms)

RESULT: Thus the monostable multivibrator is designed and its output waveform is traced.

EX.NO: ASTABLE MULTIVIBRATOR

DATE: AIM:

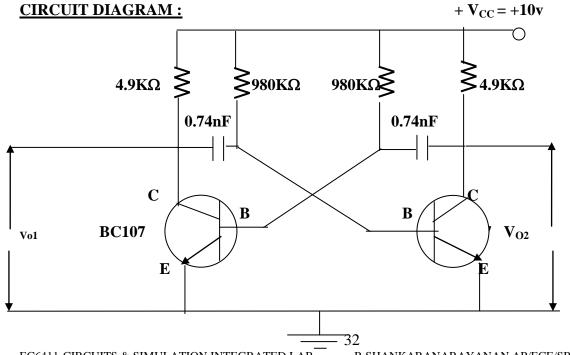
To design a astable multivibrator and study the waveform.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC107	2
2	RESISTOR	980ΚΩ	2
		4.9ΚΩ	2
3	CAPACITOR	0.74nF	2
4	RPS	(0-30) V	1
5	CRO	-	1

THEORY:

Astable multivibrator has no stable state, but has two quasi – stable states. The circuit oscillates between the states (Q1 ON, Q2 OFF) and (Q2 ON, Q! OFF). The output at the collector of each transistor is a square wave. Therefore this circuit is applied as a square wave generator. Refer to the fig each transistor has a bias resistance RB and each base is capacitor coupled to the collector of other transistor. When Q1 is ON and Q2 is OFF, C1 is charged to ($V_{cc} - V_{BE1}$) positive on the right side. For Q2 ON and Q! OFF, C2 is charged to $(V_{cc} - V_{BE2})$ positive on the left side.



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Design

Given
$$Vcc = 10V$$
; $Ic = 2 \text{ mA}$; $h_{FE} = 200$; $f = 1 \text{ kHz}$

$$R \le h_{FE} Rc$$

$$R_{C} = V_{CC} - V_{C2(sat)} \ / \ I_{C} = 10 - 0.2 \ / \ 2x \ 10^{-3}$$
 =4. 9 $K\Omega$

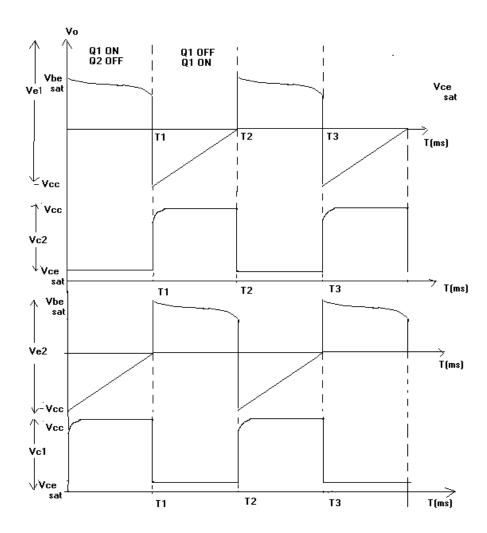
$$R \le 200 \times 4.9 \times 10^3 = 980 \text{ K}\Omega$$

$$T = 1.38 RC$$

$$1 \times 10^{-3} = 1.38 \times 980 \times 10^{3} \times C$$

$$C = 0.74 \text{ nF}$$

Waveforms:



PROCEDURE:

- 1. The connections are given as per the circuit diagram.
- 2. Switch on the power supply.
- 3. Observe the waveform both at bases and collectors of Q1 and Q2.
- 4. Connect the CRO in the output of Q1 and Q2 and trace the square waveform.

RESULT:

Thus the square wave forms are generated using a stable multivibrator.

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EX.NO: BISTABLE MUITIVIBRATOR

DATE:

AIM:

To design a bistable multivibrator and study the output waveform.

Apparatus Required:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR	4.7ΚΩ	2
		22ΚΩ	2
3	CAPACITOR	0.022μf	2
		10μf	2
		100Pf	2
4	CRO	-	1
5	RPS	(0-30) V	1
6	FUNCTION	-	1
	GENERATOR		

THEORY:

The bistable multivibrator is a switching circuit with a two stable state either Q1 is on and Q2 is off (or)Q2 is on and Q1 is off. The circuit is completely symmetrical. load resistors RC_1 and RC_2 all equal and potential

Divider (R1,R2)and $(R_1'$ and $'R_2$ ') from identical bias Network at the transistor bases. Each transistor is biased from the collector of the other

Device when either transistor is ON and the other transistor is biased OFF.C1andC2 operate as speed up capacitors or memory capacitors.

Design:

Given
$$Vcc = 12V$$
; $V_{BB} = -12v$; $Ic = 2mA$; $V_{C(sat)} = 0.2 V$

VBE(sat) = 0.7V

Assume Q1 is cut-off Vc1 = VCC(+12V)

Q2 is in saturation (ON) Vc2 = Vc(sat) (0.2 V)

Using superposition principle,

$$VB1 = VBB[R1/R1 + R2] + Vc2[R2/R1 + R2] << 0.7$$

Let us consider VB1 = -1V

Then
$$-1 = [-12R1/R1+R2] + [0.2R2/R1+R2]$$

Assume R1 = $10K\Omega$ such that it ensures a loop gain in excess of unity during the transition

between states. The inequality

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$$R2 = 91.67 \text{ K}\Omega$$

Test for conditions : Q1 = cut-off(Vc1 = 12V)

$$Q2 = Saturation / (ON) (VC2 = 0.2V)$$

Minimum base current, IB (min) must be less than the base current (IB) i.e.,

$$I_B$$
 (min) $< I_B$

Calculate h_{fe} from multimeter (say = 200)

$$\begin{split} I_{B\,2}(min) &= I_{c2}\,/\,h_{fe} \\ I_{c2} &= Ic-I3 \\ I_{c2} &= (\,2-0.12\,)mA = 1.88\,mA \\ I_{B\,2}(min) &= 1.88mA\,/\,200 = 9.4\,\mu A \\ I_{B\,2} &= I_1-I_2 \\ I_{B\,2} &= (0.71-0.14\,)mA = 0.57\,mA \end{split}$$

Since
$$I_{B2} > I_{B2}(min)$$
, Q2 is ON

$$C1 = 25 pF (Commutative capacitor)$$

$$I_C = V_{CC} - Vc_2 / R_C$$

$$R_C = V_{CC} - Vc_2 / I_C = 12 - 0.2 / 2x 10^{-3} = 5.9 \text{ K}\Omega$$

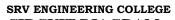
$$I_3 = Vc_2 - V_{BB} / R1 + R2 = 0.2 + 12 / (10 + 91.6)K = 0.12mA$$

$$I_1 = Vc_1 - V_{BE}/R_C + R1 = 12 - 0.7/(5.9 + 10) K = 0.71mA$$

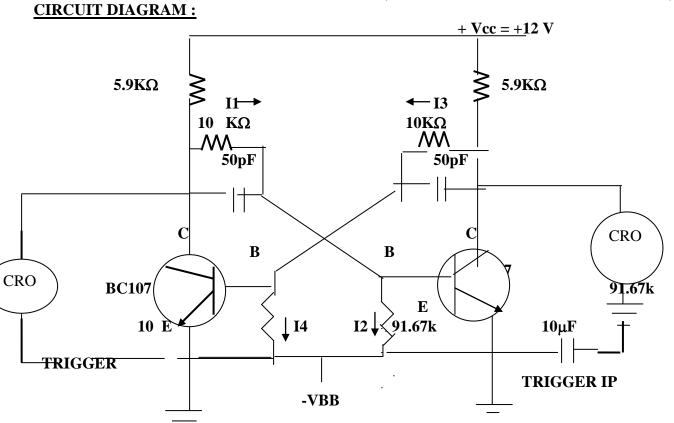
$$I_2 = V_{BE} \cdot V_{BB} / R_2 = 0.7 + 12 / 91.6K = 0.14 \text{ mA}$$

Procedure:

- 1. Connect the cir cuit as per circuit diagram.
- 2. Switch on the regulated power supply and observe the output waveform at the collector of Q1 and Q2.
- 3. Sketch the waveform.
- 4. Apply a threshold voltage and observe the change of states of Q1 and Q2.
- 5. Sketch the waveform.



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OBSERVATION:

VOLTAGE	Time Period	Frequency	Amplitude
<u>VC1</u>			
<u>Vc2</u>			

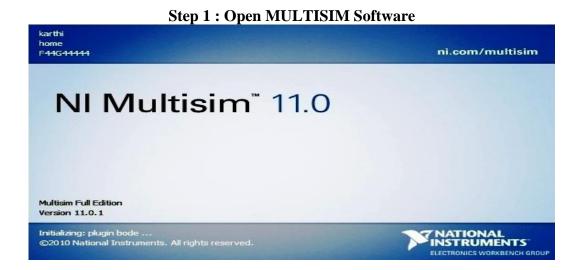
RESULT:

Thus the bistable multivibrator is designed and the square waveforms are generated at the output.

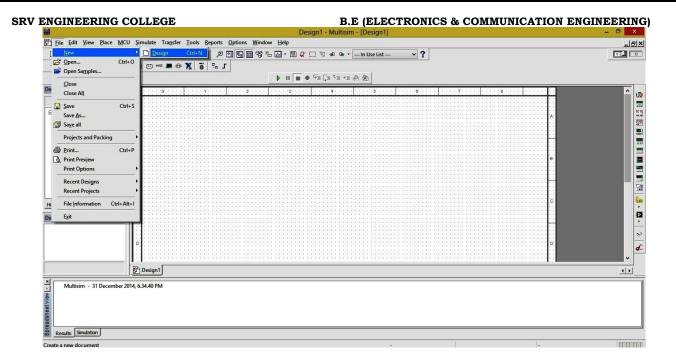
SIMULATION LAB

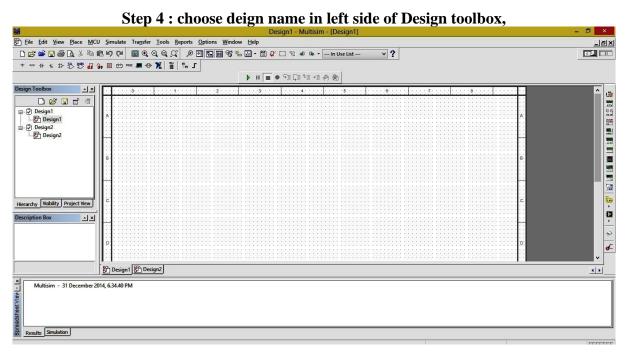
GUIDELINES FOR DESIGNING CIRCUITS IN MULTISIM

 Same procedure is for MULTISIM also only slight variations to choose components and project title. comparing with ORCAD ,MULTISIM is user friendly software to design circuits.



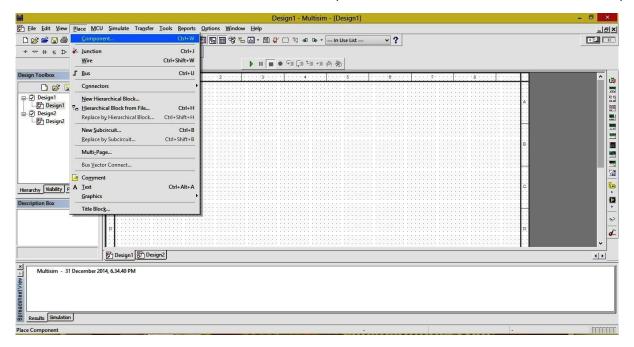
Step 3: Choose File menu ->new->Design



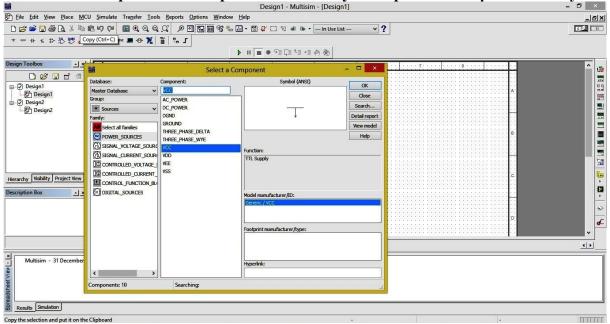


Step 5: to select component, choose place->component

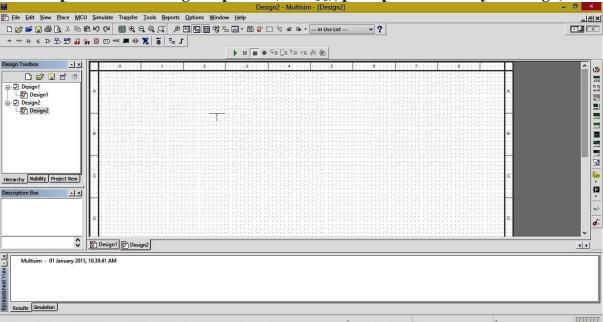
B.E (ELECTRONICS & COMMUNICATION ENGINEERING)



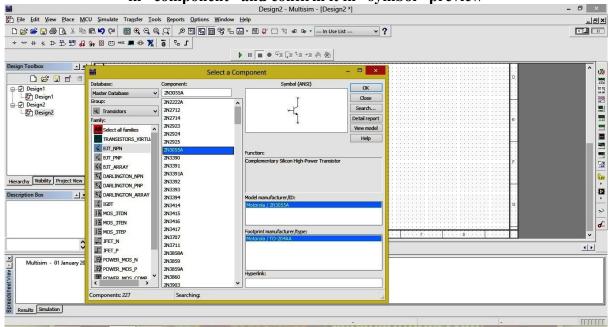
STEP 6: To select particular component click family->component->see preview in "symbol"



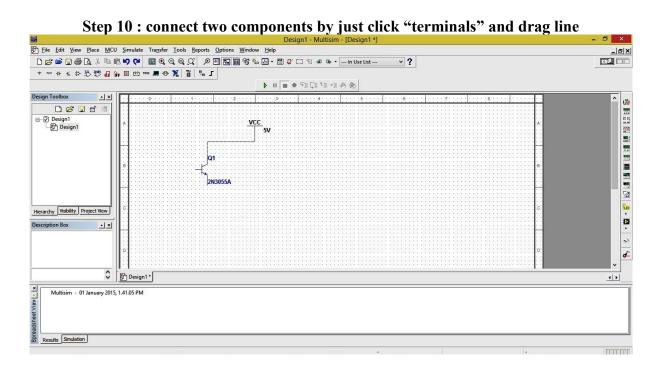
Step 7: after selecting component (ex V_{CC}), place part in PCB layout design,



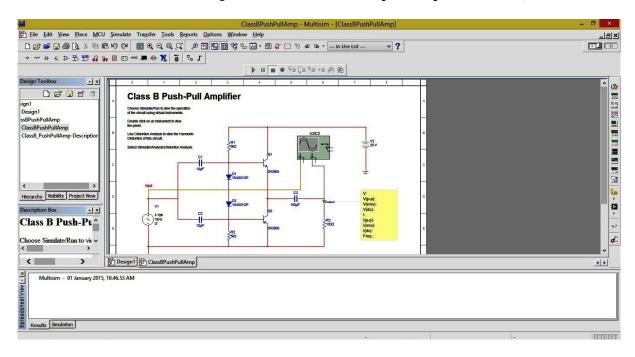
Step 8: To select BJT transistor, choose "Groups"->click "BJT_NPN" in family->choose model in "component" and confirm it in "symbol" preview



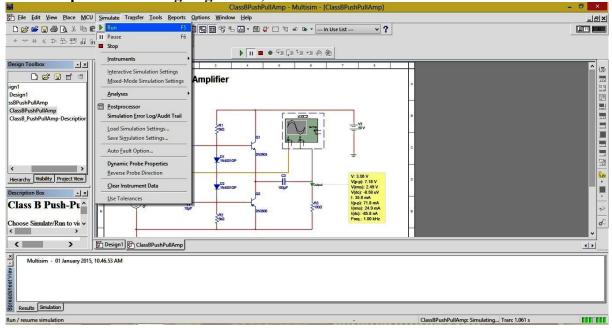
Step 9: after selecting V_{CC} and BJT place it in design, En Edit View Place MCU Simulate Transfer Tools Reports Options Window Help 그리× v ? ▶ II ■ ● FE CE *E +E @ ● Design Toolbox × Design1
Design2
Design2 VCC 5V Hierarchy Visibility Project View ď Design1 Design2* 4 > Results Simulation



STEP 11: example for "class "B" Push pull amplifier circuit,



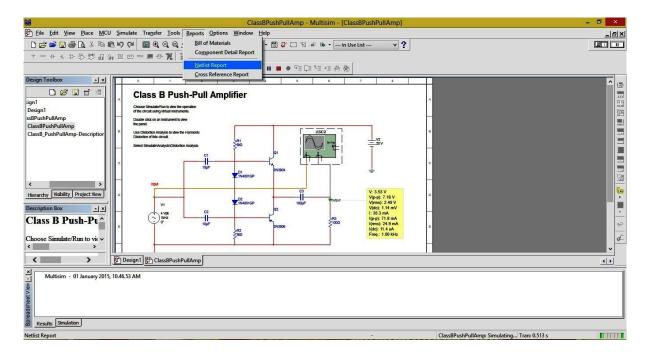
Step 12. After designing circuit, To simulate circuit click "Run" in Simulate



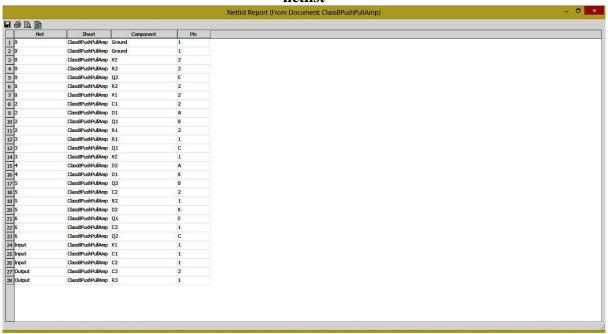
ClassBPushPullAmp - Multisim - [ClassBPushPullAmp] - 0 × En Eile Edit View Place MCU Simulate Transfer Tools Reports Options Window Help **▶ || ■ ●** FE CE tE +E 49 **&** Oscilloscope-XSC2 Design Toolbox ____x Class B Push-Pull Amplifier Design1 ssBPushPullAmp ClassBPushPullAmp Choose Simulate/Run to view the operation of the circuit using virtual instruments. Double click on an instrument to view the panel. ClassB_PushPullAmp-Description • *** Hierarchy Visibility Project View T1 + 147.981 ms T2 + 147.981 ms T2-T1 0.000 s Reverse Description Box 4 Vpt 10012 0" Class B Push-Pu^ Trigger
Edge: Ft A B Ext
Level: 0 V Timebase Scale: 200 us/Div Scale: 2 V/Div Scale: 2 V/Div Choose Simulate/Run to vic v Y pos.(Div): 0 Y pos.(Div): 0.6 Y/T Add B/A A/B AC 0 DC < Design1 ClassBPushPullAmp Multisim - 01 January 2015, 10.46.53 AM Results Simulation ClassBPushPullAmp: Simulating... Tran: 0.149 s

Step 13: To see output, click in "CRO" to see output,

Step 14: for example netlist for class "B" push pull amplifier look likes



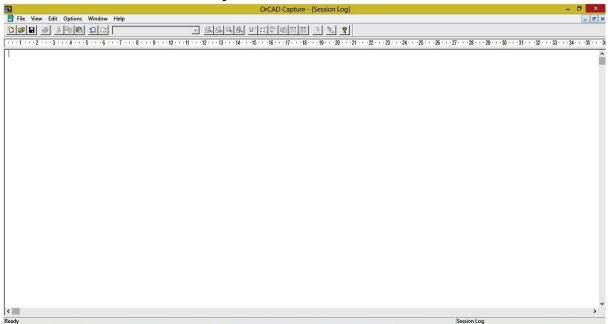
Step 15 : You can run circuit by design 'NETLIST' in report option, to see netlist click "reports"-netlist

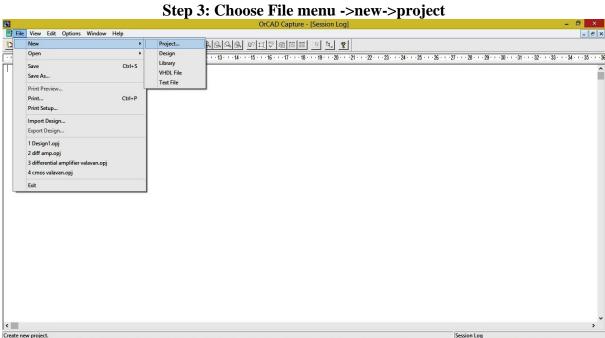


GUIDELINES FOR DESIGNING CIRCUITS IN PSPICE

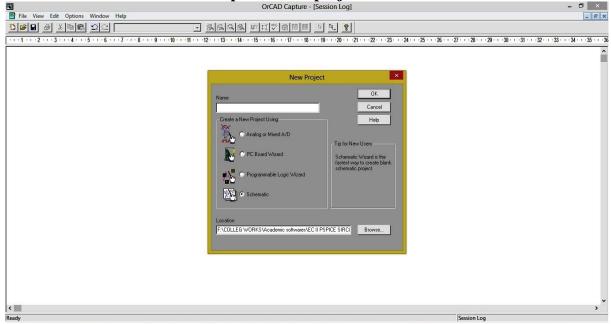


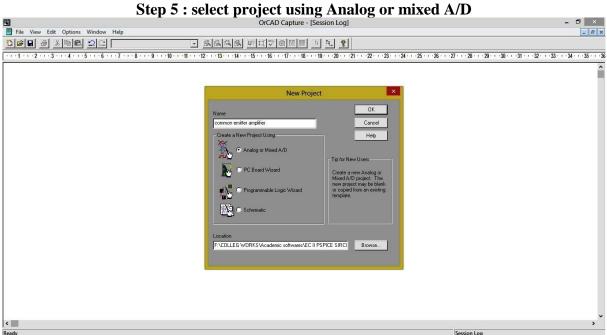
Step 2: ORCAD main window



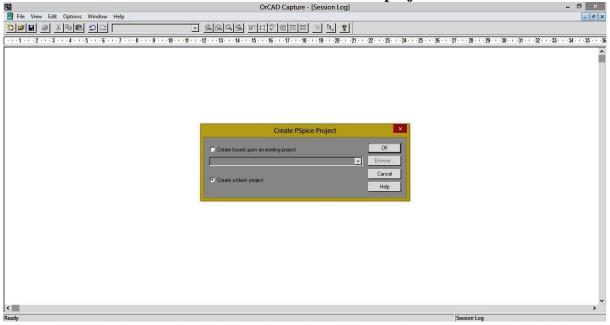


Step 4 : choose project name

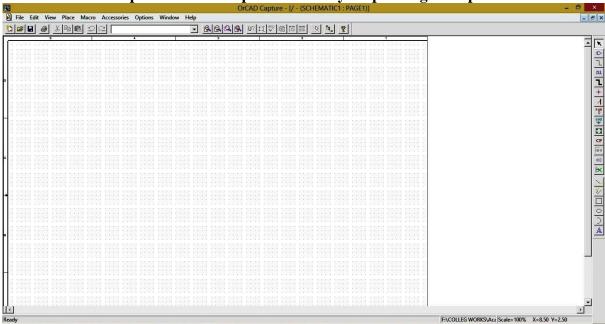




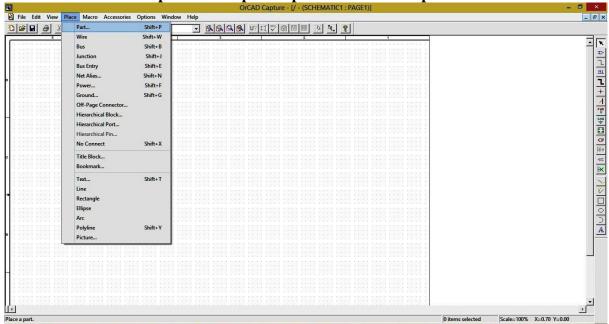
STEP 6 : Choose create blank project



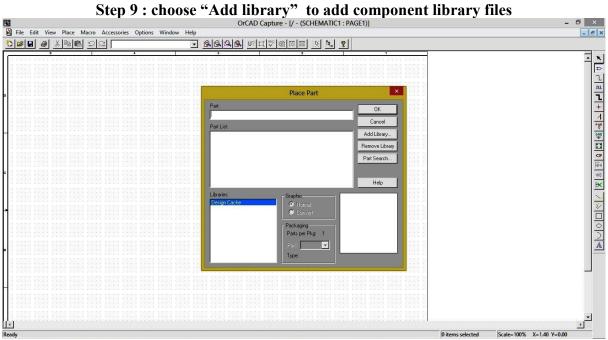
Step 7 : ORCAD capture PCB Layout pin diagram opens



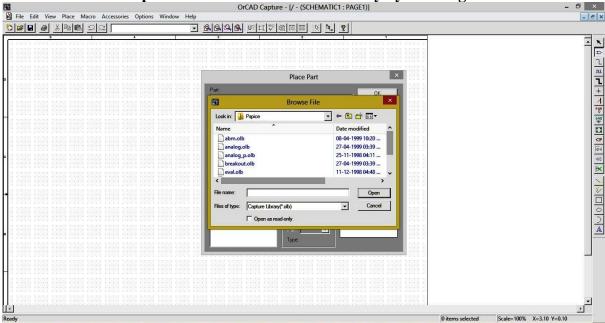
Step 8 : choose place->part-to choose components



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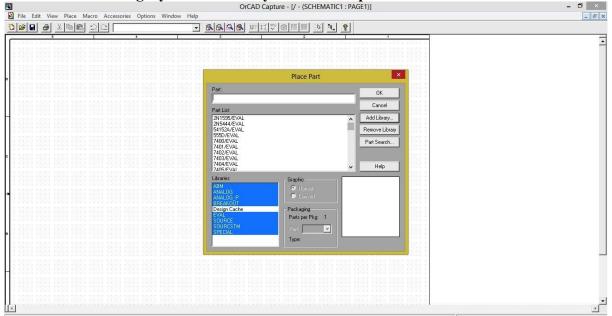
 $\textbf{Step 10: Add all files to main memory by selecting all} \\ \text{\tiny OrCAD Capture - [/-(SCHEMATIC1: PAGE1)]}$



B.E (ELECTRONICS & COMMUNICATION ENGINEERING)

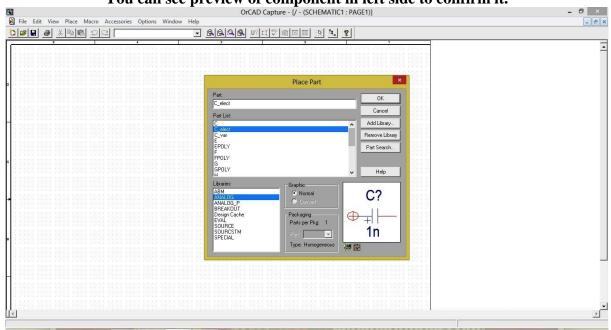
STEP 11 : Choose "category "from Library and select " part list" for to choose different elements

Orcad Capture - [/- (SCHEMATIC1: PAGE1)]

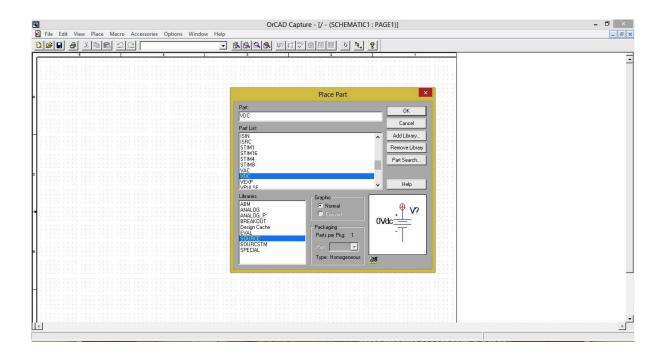


Step 12: for example to choose capacitor, select "Analog" from library and click "C" in part list.

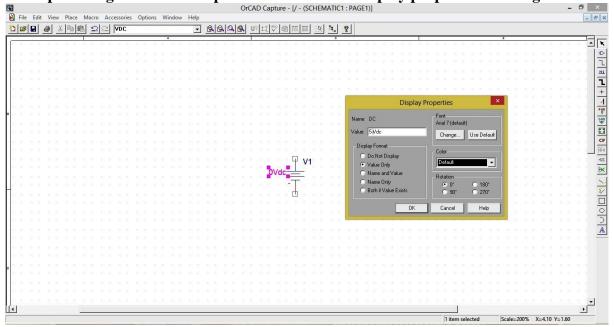
You can see preview of component in left side to confirm it.



Step 13 : to select " V_{DC} " source choose " source" from library and select it from part list, you can change it values

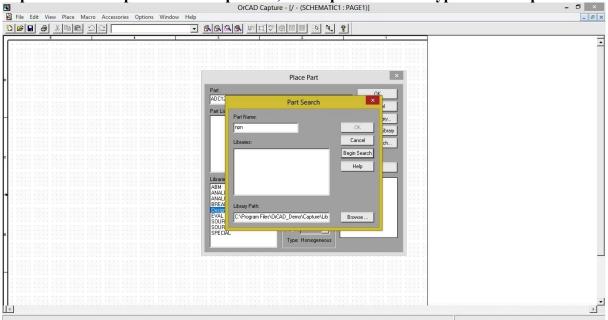


Step 14: Right click in component and -> edit -> display properties-> change value

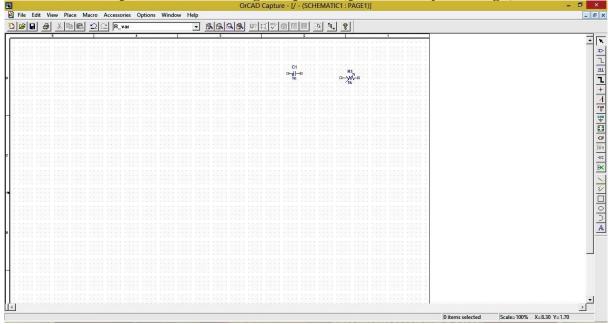


B.E (ELECTRONICS & COMMUNICATION ENGINEERING)

Step 15: to search particular component ,select "part search"->type name in "part name"

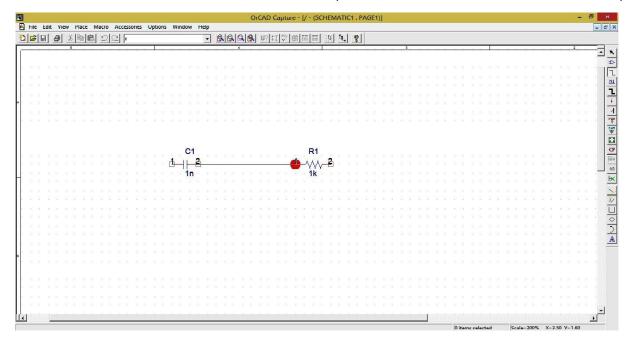


Step 16: After selecting component, place it in layout design,

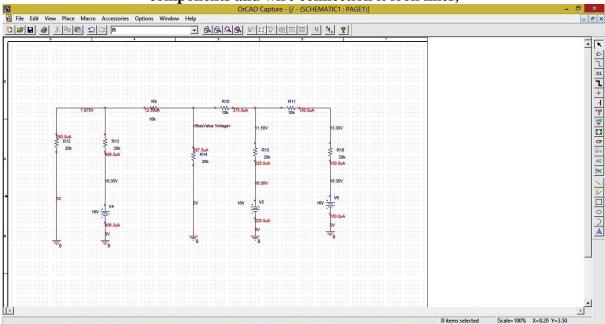


Step 17: connecting two components using "wire" by selecting wire in parts,

B.E (ELECTRONICS & COMMUNICATION ENGINEERING)



Step 18: to construct D TO A converter ,we need resistors and capacitors . after selecting components and wire connection it look likes,



Step 19: to select already designed projects, choose file->open->design->browse stored folder.

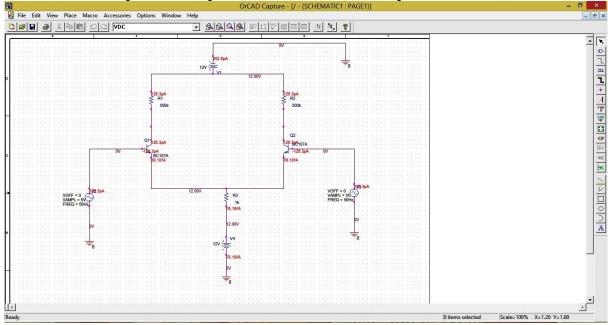
B.E (ELECTRONICS & COMMUNICATION ENGINEERING)

After click file->design sources->schematic->page1 to view designed circuits

OrCAD Capture - (differential amplifier valavan)

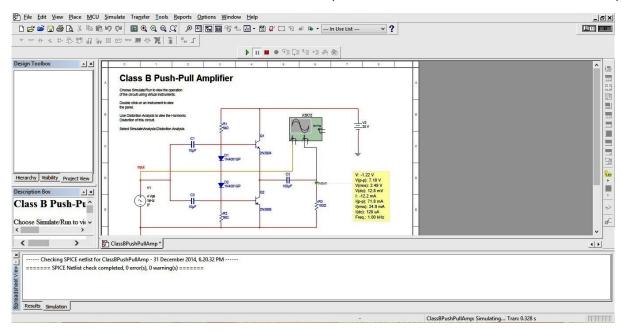
Analog or Mineré A/D



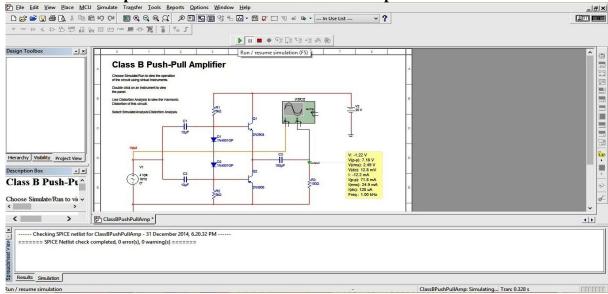


Step 21: Example for "Class "B" Push Pull Amplifier circuit,

B.E (ELECTRONICS & COMMUNICATION ENGINEERING)

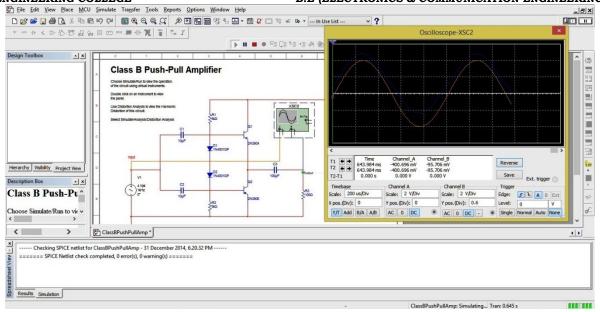


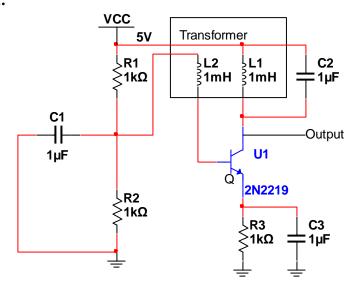
Step 22: To run simulation choose Run option and simulate



Step 23 : you can see output in CRO by selecting from parts and place it where you have to see output

B.E (ELECTRONICS & COMMUNICATION ENGINEERING)





Ex. no:

Date:

SPICE SIMULATION OF TUNED COLLECTOR OSCILLATOR

Aim:

To simulate a Tuned collector oscillator circuit and to plot the frequency response characteristics.

Apparatus required:

- i)Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

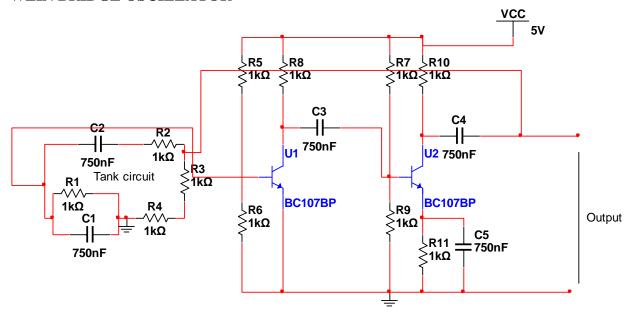
- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

Result:

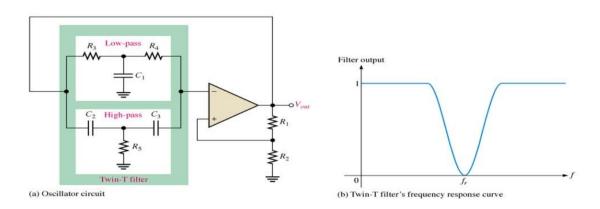
Thus the Tuned collector oscillator is simulated successfully.

Circuit Diagram:

WEIN BRIDGE OSCILLATOR



TWIN T OSCILLATOR:



Ex.	no:
Dat	e:

SPICE SIMULATION OF WEIN BRIDGE AND TWIN T OSCILLATOR

Aim:

To simulate a Wein Bridge and Twin T oscillator circuit and to plot the frequency response characteristics.

Apparatus required:

- i)Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

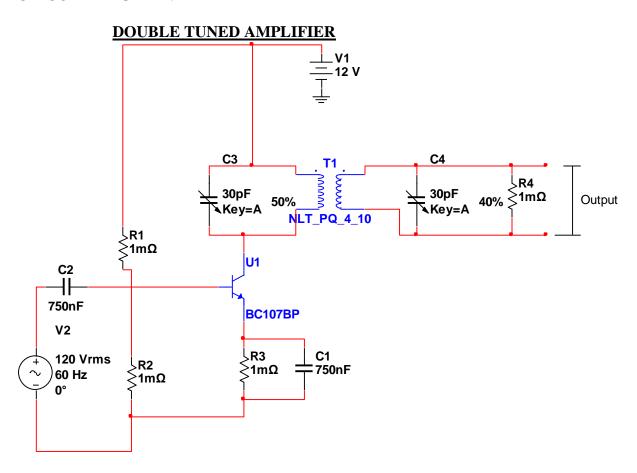
Procedure:

- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

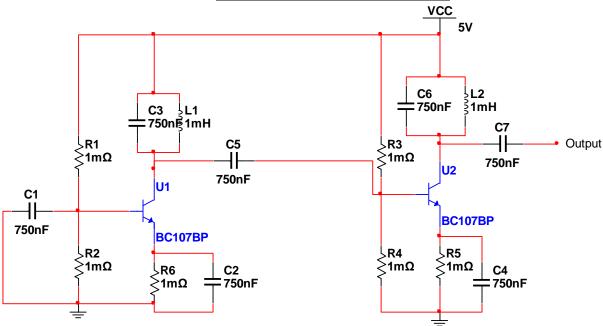
Result:

Thus the Wein Bridge and Twin T oscillator circuit is simulated successfully.

60



STAGGER TUNED AMPLIFIER



EC6411-CIRCUITS & SIMULATION INTEGRATED LAB

R.SHANKARANARAYANAN,AP/ECE/SRVEC

Ex.	no
Dat	۰.

SPICE SIMULATION OF DOUBLE AND STAGGER TUNED AMPLIFIERS

Aim:

To simulate a Double and Stagger tuned Amplifiers circuit and to plot the frequency response characteristics.

Apparatus required:

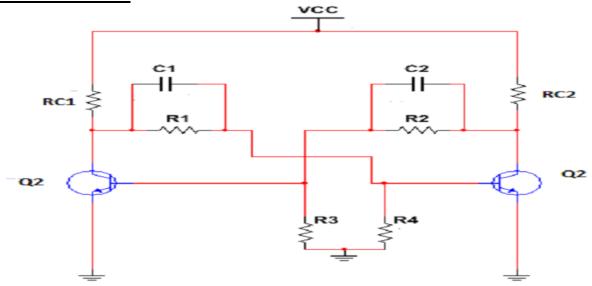
- i) Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

Result:

Thus the Double and Stagger tuned Amplifier were simulated successfully.



BI STABLE MULTIVIBRATOR

Ex. no: Date:

SPICE SIMULATION OF BI STABLE MULTIVIBRATOR

Aim:

To simulate a Bistable Multivibrator circuit and to plot the frequency response characteristics.

Apparatus required:

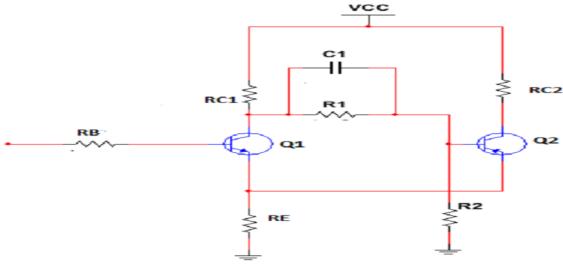
- i) Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

Result:

Thus the Bistable Multivibrator was simulated successfully.



SCHMITT TRIGGER

Ex. no: Date:

SPICE SIMULATION OF SCHMITT TRIGGER

Aim:

To simulate a Schmitt trigger circuit and to plot the frequency response characteristics.

Apparatus required:

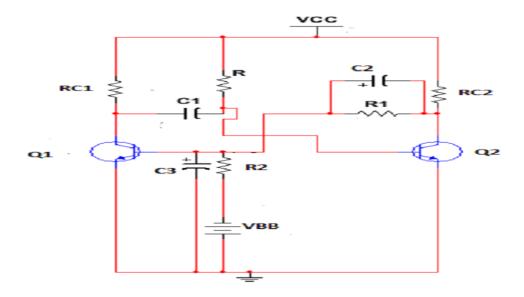
- i) Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

Result:

Thus the Schmitt Trigger was simulated successfully.



MONO STABLE MULTIVIBRATO

Ex. no: Date:

SPICE SIMULATION OF MONO STABLE MULTIVIBRATOR

Aim:

To simulate a Mono stable Multivibrator circuit and to plot the output characteristics.

Apparatus required:

- i) Personal Computer
- ii) **SPICE** (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

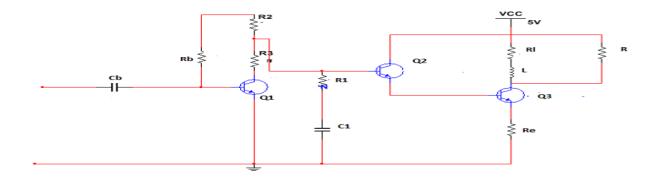
- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.
- vi) The VI graph is observed in the Waveform Viewer

Result:

Thus the Mono stable multivibrator was simulated successfully

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CURRENT TIME BASE GENERATORS

Ex. no: Date:

SPICE SIMULATION OF CURRENT TIME BASE GENERATORS

Aim:

To simulate a Current time base circuit and to plot the output characteristics.

Apparatus required:

- i) Personal Computer
- ii) SPICE (PSPICE 9.0 v& above or MULTISIM 10.0 v & above) Software.

Procedure:

- i) Draw the circuit diagram after loading components from library.
- ii) A DC source with 0 V is place as the dummy voltage source to obtain the current waveform.
- iii) Wiring and proper net assignment has been made. The circuit is preprocessed. The VI characteristics may be obtained by performing DC transfer function Analysis. Place the current waveform marker at the positive terminal of the dummy voltage source (voltage =0 volts).
- Iv) For placing waveform markers, select tools instruments set wave form conent current waveform click on the required net and place the waveform marker. The sweep parameter (voltage) for input source is set in the Analysis window.
- V) The applied voltage is swept from an initial value to final value with the steps provided To get VI characteristics, the currents corresponding to varying input voltages are noted.

Result:

Thus the Current time base circuit was simulated successfully.